PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-209124

(43)Date of publication of application : 28.07.2000

(51)Int.Cl. H04B 1/707
H04L 7/00

(21)Application number : 11-006217

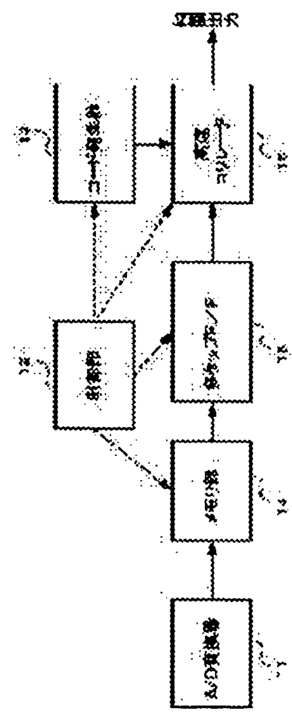
(22)Date of filing : 13.01.1999

(71)Applicant : KOKUSAI ELECTRIC CO LTD

(72)Inventor : IMAIZUMI ICHIRO
HOSHINA TAKAYA
YASUNARI KENJIRO

(54) CORRELATION CIRCUIT FOR SPREAD SPECTRUM COMMUNICATION

(57)Abstract:



PROBLEM TO BE SOLVED: To provide a correlation circuit for spread spectrum communication to obtain a correlation regardless of an inexpensive LSI whose component scale is made small.

SOLUTION: An A/D converter 11 converts a received signal that is spread- spectrum-processed into a digital signal, which is written by one symbol to a memory circuit 14 on the basis of clock signal equal to or higher by over- sample a chip rate of the CDMA under the control of a control section 12, a multi-tap F/F 15 reads information from the memory circuit 14 at a high speed in multi-tap to conduct parallel/serial conversion (time conversion) and a high speed correlator 16 and a delay F/F are used to conduct a cross product arithmetic operation at a high speed in this correlation circuit for spread spectrum communication.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

F/F(

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the correlator for spread spectrum systems used by the receiver side of the spectrum diffusion communication system in mobile communications, wireless LAN, etc., and relates to the correlator for spread spectrum systems of an easy and small-scale configuration especially.
[0002]
[Description of the Prior Art] In the spectrum diffusion (Spread Spectrum:SS) communication system generally used for mobile communications or wireless ~~LAN,~~ two steps of modulations which perform a narrow-band modulation (primary modulation) to transmit data by the transmitting side, and perform a diffusion modulation (secondary modulation) further are performed, data are transmitted, and by the receiving side, after performing the back diffusion of electrons to received data and returning to a primary modulation, baseband signaling is reproduced in the usual detector circuit.
[0003] And the correlator for spread spectrum systems which acquires the correlation for restoring to the input signal by which SU ** KUTORAMU diffusion was carried out conventionally consists of a back-diffusion-of-electrons circuit and a demodulator circuit of a sign division multiplex modulated wave, and the correlator for spread spectrum systems performs synchronous prehension, and concretely, in order to take correlation with the synchronous phase detected after that, the slide correlator (SC) which consisted of logical circuits is used.
[0004] If a slide correlator shifts 1 bit (diffusion sign) of sign sequences from a station at a time using 1-bit correlator, correlation with the sign sequence of reception is searched for each time and correlation is searched for about the number of bits of only sign sequence length, the synchronous phase from which correlation serves as a peak will be called for, and synchronous prehension will be performed.
[0005] Here, the slide correlator which is one of the conventional back-diffusion-of-electrons circuits is explained using drawing 9 . Drawing 9 is some configuration block Figs. of the conventional slide correlator. The part which acquires the correlation output in the conventional slide correlator consists of A/D converter 31, the multiplier 32, a PN code register 33, an adder 34, and a delay circuit 35.
[0006] Each part of the above-mentioned conventional slide correlator is explained. A/D converter 31 is a highly precise analog-to-digital converter which changes into a digital signal the analog signal which the sign division multiplex (Code Division Multiple Access:CDMA) modulation was carried out, was transmitted, and was received with the antenna (not shown). The PN code register 33 is a register which outputs PN (Pseudo Random Noise) sign code which is the same diffusion sign as having been used for the CDMA modulation by the transmitting side.
[0007] A multiplier 32 is a multiplier which carries out the multiplication of the PN code outputted to the digital received data outputted from A/D converter 31 from the PN code register 33. An adder 34 and a delay circuit 35 carry out 1 symbol period accumulation of the multiplication result outputted from a multiplier 32, and output the integral value as a correlation output.
[0008] The analog signal of the received data received with the antenna is changed into a digital signal

with A/D converter 31, multiplication is carried out with the PN code and multiplier 32 which are outputted from the PN code register 33, accumulation of the actuation of the conventional slide correlator is carried out to an adder 34 in a delay circuit 35, and the addition result for one symbol is outputted as a correlation output. And multiplication and accumulation are repeated 1 chip ** carrying out timing of the multiplication in a multiplier 32, and changing a phase, and the synchronous phase from which a correlation output serves as a peak is detected.

[0009] The configuration using a slide correlator as this back-diffusion-of-electrons circuit is comparatively simple, and that there is [therefore] little gate number, although it is said that there is little power consumption, generally time amount until it performs synchronous prehension has the problem of taking time amount until it obtains a correlation output only several chip minutes in the time amount x1 symbol for one symbol for this reason.

[0010] In order to solve the trouble of taking time amount before obtaining a correlation output, it considers using a matched filter (a matched filter or Matched Filter:MF) for the correlator for spread spectrum systems instead of the slide correlator. A matched filter performs synchronous prehension in 1 symbol time amount by taking the correlation at the time of shifting a phase all at once.

matched filter

[0011] Here, the matched filter which is another example of the conventional back-diffusion-of-electrons circuit is explained using drawing 10. Drawing 10 is the block diagram showing the example of a configuration of the conventional matched filter. The conventional matched filter consists of A/D converter 41, the multiplier 42, a PN code register 43, an adder 44, and a sample hold (S/H) circuit 45.

[0012] Each part of the above-mentioned conventional matched filter is explained. A/D converter 41 is a converter which changes into a digital signal the input signal of the analog by which the CDMA modulation is carried out. The sample hold (S/H) circuit 45 is a circuit which are prepared, has incorporated the digital signal from A/D converter 41 one by one, and is held. [two or more]

[0013] The PN code register 43 is a register which outputs the PN code (code) which is a diffusion sign. A multiplier 42 is a multiplier which carries out the multiplication of the PN code from the PN code register 43 to the digital signal held in each sample hold circuit 45. An adder 44 is an adder which add the output from a multiplier 42 all at once.

[0014] Sequential maintenance of the input signal to which digital conversion of the actuation of the conventional matched filter was carried out with A/D converter 41 is carried out in two or more S/H circuits 45, the multiplication of the output from the S/H circuit 45 and the PN code outputted from the PN code register 43 is carried out with a multiplier 42, they add the multiplication result in a multiplier 42 all at once with an adder 44 further, and an addition result is outputted. A correlation output is obtained from the addition result.

[0015] However, in the general matched filter, to the slide correlator which takes the correlation at the time of shifting phases all at once and which carried out the sake, for example, the above-mentioned explanation, the gate number several times the chip in 1 symbol of this is needed, a gate scale increases, increase of an LSI price and increase of power consumption are caused, and for using for the receiver of a migration terminal, it has become **** as a matter of fact.

[0016]

[Problem(s) to be Solved by the Invention] Thus, with the conventional slide correlator, there was a problem of taking time amount until a correlation output is obtained, and with the conventional matched filter, the gate number increased and there was a trouble of bringing about increase of an LSI price and increase of power consumption.

[0017] In view of the above-mentioned actual condition, it succeeded in this invention, and it makes a configuration element number small-scale, and low-pricing of LSI is attained and it aims at offering the correlation circuit for spread spectrum systems which can obtain a correlation output.

motivation

[0018]

[Means for Solving the Problem] This invention for solving the trouble of the above-mentioned conventional example It stores in Boolean part which writes the input signal by which spectrum diffusion was carried out in memory, reads the written-in signal from memory to many taps according to time amount converted quantity, and performs time amount conversion. Since it is the correlation circuit

* NOTICES *

MEANS

[Means for Solving the Problem] This invention for solving the trouble of the above-mentioned conventional example It stores in Boolean part which writes the input signal by which spectrum diffusion was carried out in memory, reads the written-in signal from memory to many taps according to ~~time amount converted quantity, and performs time amount~~ conversion. Since it is the correlation circuit for spread spectrum systems which repeats the processing which performs parallel/serial conversion at a high speed in Boolean part, performs time amount conversion, and performs a diffusion sign and a sum-of-products operation at a high speed from the drawing speed of memory two or more times, a configuration element number can be made small-scale and a correlation output can be obtained.
[0019]
[Embodiment of the Invention] It explains referring to a drawing about the gestalt of operation of this invention. ~~The correlation circuit for spread spectrum systems~~ concerning the gestalt of operation of this invention About the signal which is sent out from a receive section and by which spectrum diffusion was carried out, usually The place currently processed by the diffusion sign with the so-called chip time interval Boolean part for time amount conversion reads the signal which memorizes temporarily the signal by which spectrum diffusion was carried out in the memory section, and was memorized and by which spectrum diffusion was carried out to a high speed from the memory section by two or more taps. It enables it to repeat the processing which performs the sum-of-products operation of the signal and diffusion sign which were read at a high speed two or more times, a configuration element number can be made small-scale, and a correlation output can be obtained.
[0020] Time amount conversion of the signal which is carrying out a sum-of-products operation, and is inputted into a diffusion sign and a high speed from a receive section and by which spectrum diffusion was carried out is realized specifically storing the signal by which spectrum diffusion was carried out in memory by at least 1 symbol, storing it in Boolean part for time amount conversion, and reading it further at high speed.
[0021] The chip rate of the so-called W-CDMA (wideband CDMA) proposed from ARIB (Association of Radio Industries and Businesses) by current and IMT2000 is 4M(megger) cps (chipper second). On ~~the other hand, if the manufacture~~ process of LSI in 2001 (large-scale integrated circuit) that W-CDMA is put in practical use is used, ~~in the case of CMOS (complementary MOS)~~, line breadth is set to about 0.18 micrometers, and, as for the clock frequency to be used, 500MHz to 2G(G) Hz is expected.
[0022] That is, compared with the frequency of an input signal, ~~far high processing becomes~~ possible in a circuit. Although it is necessary to mince a signal by this sampling of about 4 times from on signal processing, and to observe matching with a diffusion sign to a precision more since chip rates are 4Mcps (es) The clock still used for processing of an input signal will be processed by 16MHz, and if 1.6GHz becomes ~~usable as a clock rate of the clock used for~~ internal processing of another side and a circuit, internal processing will be equipped with a 100 times as many throughput as this to processing of an input signal.
[0023] When making the same function as a matched filter attain, the signal which was received by the 16MHz unit and by which spectrum diffusion was carried out is accumulated in memory as usually

carried out, it is read at the high speed of 1.6GHz, and if the slide correlator of high-speed processing performs a sum-of-products operation at a high speed, it can process by one 100 times the rate of this. Therefore, since 100 sample existence will be recognized by over sampling technique 4 times if it is the case where the number of chips (diffusion coefficient) is 25, it becomes possible to take correlation of one symbol by the same 1 symbol time amount as a matched filter.

[0024] In this case, although a diffusion code is repeatedly used 100 times without making it change by one symbol, the signal by which spectrum diffusion was carried out has the need of making it sliding by 1 sample unit, and it is necessary to prepare it by at least 2 symbols as memory.

[0025] First, if a part for one symbol is written in the 1st memory by 16MHz, while performing a part for the one following symbol for every sample and writing in the 2nd memory, you make it slide one sample of data for one symbol at a time by 1.6GHz from the 1st and 2nd memory, and read-out is performed 100 times.

[0026] That is, making it slide one sample of data for one symbol at a time from the 1st memory in which the data for one symbol were written, and the 2nd memory by which it succeeds in writing for every sample, and performing read-out 100 times by 1.6GHz About the 2nd memory, writing and read-out will be performed to coincidence, and the signal with which spectrum diffusion of [for the one just following symbol] was carried out will be read into the time amount which reads the data for one symbol by the 2nd memory. If this actuation is performed by turns by the 1st memory and 2nd memory, the writing to the memory of the signal by which spectrum diffusion was carried out continuously, and read-out can be operated. Therefore, it becomes possible like a matched filter to always send out a correlation output.

[0027] In the case of W-CDMA, the above-mentioned diffusion coefficient changes with physical channels, but it is necessary four chips at the lowest, and it is [256 chip] necessary at the maximum. However, you may think that a chip rate is fixed at 4.096Mcps(es) in this case. In addition, it may rise in the future to 16.384Mcps(es) the adjustable rates are assumed to be. Therefore, when it needs [256 chip] at the maximum, with the slide correlator (high speed SC) of high-speed processing of a piece, it can process actually. In that case, what is necessary is to prepare two or more high speeds SC, to shift one sample of same operations at a time, and just to perform them.

[0028] Since it becomes 1024 samples (256 chip x4 over sampling technique) in the case of 256 chips, as a data read-out clock from memory, a 1.6GHz clock is usable, and specifically, that needs the high speed SC of 11 pieces in order to perform processing of being 100 times many as this, with a 1.6GHz clock. Correspondence to 1100 samples (100 sample x11 piece) is attained at the high speed SC of 11 pieces. Even in this case, if compared with the hard scale which constitutes the matched filter (MF) of 1024 taps, it can realize on a scale of [few / far] hard.

[0029] However, in the above-mentioned circuit, since a hard scale is larger than 1/100, power consumption will become large that the rate has increased 100 times compared with MF. However, it is effective in reducing LSI cost that the MF section which occupies the great portion of recovery section of W-CDMA becomes about 1/10 since a hard scale becomes about 1/10.

[0030] In addition, although the above-mentioned example explained the case where a diffusion sign was not exchanged, the signal is fixed and it becomes possible to specify a diffusion sign for a short time, and to obtain a correlation output, if it performs exchanging a diffusion sign.

[0031] Moreover, if the sum-of-products computing element of MF configuration is prepared instead of a high speed SC and read-out from memory is performed to it by the many taps of a symbol unit, it will become possible to output the correlation output to the case of a short time, for example, a 1GHz clock, in 1ns (nanosecond) extremely. This is effective, when preparing much memory, accumulating the information on many symbol units in these memory and obtaining the correlation output. That is, if it is original, even when two or more MF is required, processing will become possible at one MF.

[0032] In addition, when going for the thing whose MF actuation is the need as a migration terminal to catch the long mask symbol of the first perch [1st] among initial synchronizations in a W-CDMA system that is, it is only at the symbol synchronization and slot synchronous establishment time, and has become the gestalt allowed intermittent actuation except it. An initial synchronization specifies a long

code group as the long mask symbol of the 2nd perch, after catching the long mask symbol of this first perch. This can be attained by restoring to the input signal at the time of the same in another short code. Furthermore, a long code is specified in the location of the pilot symbol of the first perch. Thereby, an initial synchronization can be attained about.

[0033] The line is made into less than 3 seconds for the time amount which must complete these actuation to two or more base stations in these actuation. The time amount which goes to catch an early long mask symbol in this is in between (less than at least 1 second) very for a while, and if it takes into consideration that only the time of switching on performs the above-mentioned actuation to the whole duration of a call even if power consumption becomes large here, it can be said that most effects to a cell cannot be found. That is, it becomes that what is necessary is just to usually perform SC actuation intermittently, and reduction of power consumption can also be attained synthetically.

[0034] It is necessary to perform read-out from memory at a high speed from drawing speed in the circuit mentioned above. In the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention, the read-out rate from memory presupposes that it is the same as drawing speed, however reads to multi-tap (many samples) coincidence.

[0035] It carries out that it is equivalent to high-speed read-out memory by storing this in Boolean part for time amount conversion of a F/F configuration (flip-flop configuration), and performing read-out from here at high speed.

[0036] Next, the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention is explained using drawing 1 . Drawing 1 is the configuration block Fig. of the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention. In addition, the actuation (at the time [Usually] of a communication link) after the symbol synchronization with actuation simple first comparatively, a wireless slot synchronization, and frame synchronization are established is explained here. The correlation circuit for spread spectrum systems of the gestalt of this operation (this circuit) The code generator 13 which generates the PN code (PN code) of time series as shown in drawing 1 , A/D converter 11 which inputs the spectrum diffusion signal modulated by the PN code, and changes the analog signal into a digital signal, and the memory section 14 holding the digital signal, Multi-tap F/F15 which reads and holds data from the memory section 14, The high-speed correlator 16 which carries out sum-of-products data processing of the output from multi-tap F/F15, and the PN code outputted from the code generator 13 to a high speed, It consists of control sections 12 which control I/O of the data to the memory section 14, multi-tap F/F15, the code generator 13, and the high-speed correlator 16 etc.

[0037] Usually, actuation of this circuit at the time of a communication link is explained. The memory section 14 plays the role of the memory which holds the digital signal inputted temporarily, and can hold the data for one symbol now. And it incorporates in the memory section 14 with directions of a control section 12, carrying out the sequential shift of the data for one symbol of a signal from a head sample. Here, since it is premised on a symbol synchronization, a wireless slot synchronization, and frame synchronization being established, it is turned out in which phase the head sample of a specific symbol exists.

[0038] A control section 12 makes it read to multi-tap F/F15 by many taps (many samples) to the memory section 14 at the same rate as an old incorporation rate (if it to be the usual 4 time over sampling technique about 16MHz, correctly 4 4.096MHz times), i.e., a sample rate.

[0039] And multi-tap F/F15 performs parallel/serial conversion at a quick rate compared with the rate read by many taps, and outputs it to the high-speed correlator 16. This parallel/serial conversion means time amount conversion, and a conversion output rate is defined by the precision of multi-tap F/F15, the number of over sampling techniques, and the number of the high-speed correlators 16. In the example of drawing 1 , the case where the number of the high-speed correlators 16 is one is shown, and the number N of taps of multi-tap F/F15 is set to 1024.

[0040] Moreover, when outputting for example, at a rate 16 times the rate of the signal inputted into multi-tap F/F15, the number N of taps is 16, and if an input signal is inputted by 16Mcps(es), an output signal will be outputted at the rate of 16 McpsxN(16) =256Mcps. In this case, when the number of over

16 times

sampling techniques is set to 4, it is set to 256Mcps/4=64 and 64 high-speed correlators 16 are needed.
[0041] In response to the output, the high-speed correlator 16 performs a sum-of-products operation with the clock of the same rate as the read-out rate of multi-tap F/F15. At this time, a diffusion sign (PN code) is received with the sequential above-mentioned clock rate from the code generator 13. Here, the code generator 13 may be a code register. the control section 12 same also as generating and read-out of this sign -- therefore, it is controlled. In addition, the multiply operation in which it succeeds with the high-speed correlator 16 will output the data (many bits) from the memory section as it is, if a diffusion sign is "1", and if a diffusion sign is "0", it will output reversal of many bits.
[0042] Next, the case where two or more high-speed correlators 16 have is explained using drawing 2 . Drawing 2 is the configuration block Fig. of the correlation circuit for spread spectrum systems of the complex mold concerning the gestalt of operation of this invention. In addition, although it is omitting in order to simplify the control section 12 and the code generator 13 which are shown by drawing 1 , like drawing 1 , a control section 12 controls the memory section 14, multi-tap F/F15, the high-speed correlator 16, and the I/O timing to delay F/F17, and the code generator 13 outputs a diffusion code to the high-speed correlator 16.
[0043] A/D-converter 11a by which the circuit of a complex mold changes the Q signal of an input signal into digital one from an analog as shown in drawing 2 , A/D-converter 11b which changes the I signal of an input signal into digital one from an analog, The memory section 14 which memorizes the digital signal from A/D converters 11a and 11b, Multi-tap F/F 15a and 15b which carries out parallel/serial conversion of the digital signal inputted from the memory section 14, It consists of two or more high-speed correlators 16 which perform a correlation operation in response to the output of two or more delay F/F17 which is made to carry out sequential delay and outputs the digital signal from multi-tap F/F15, and multi-tap F/F15, and the output from delay F/F17. In addition, delay F/F17 constitutes the delay section, in the high-speed correlator 16, it has the multiplication section which succeeds in multiplication with a diffusion sign (diffusion code), and all the outputs from further two or more high-speed correlators 16 are added, and the whole correlation output is obtained. However, in drawing 2 , the adder unit for obtaining the whole correlation output is not illustrated. While having formed two multi-tap F/F15 is writing in by one here, one more is for reading and it is for performing this actuation by turns.
[0044] Although the read-out rate in the memory section 14 is the same as drawing speed, when reading, it reads many measurement sizes. After multi-tap F/F15 inputs many measurement sizes into parallel and carries out serial conversion from the memory section 14, it is outputted to the high-speed correlator 16 or delay F/F17. The part which operates at high speed by performing parallel/serial conversion (time amount conversion) by this multi-tap F/F15 turns into only a part which consists of digital circuits.
[0045] By considering as a configuration like drawing 2 , it becomes usable about full-scale memory, such as DRAM or SRAM, and reduction of a chip area and reduction of a chip price are attained. Moreover, like drawing 7 , a high-speed correlator (SC) can be arranged in the shape of a matrix, and the recovery of two or more users' information can be enabled. Drawing 7 is the configuration block Fig. of the correlation circuit for spread spectrum systems which the gestalt of operation of this invention requires and in which a multiple user recovery is possible. In this case, SC can be operated now only to the timing of required receipt information, and the function as a searcher can also be given to SC train, and the operation number of bits can be reduced in this case.
[0046] Below, the relation of the number of memory at the time of constituting the conversion time (multiple) in the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention, a clock frequency (Hz) of operation, the number of high-speed correlators (SC), and the memory section from F/F, the number of delay F/F, and the number of multi-tap F/F (F/F for time amount conversion) is shown in [Table 1].
[0047]
[Table 1]

変換時間	クロック周波数	SC数	メモリ部のF／F数	遅延F／F数	時間変換用F／F数
1	16M	1024	0	2048	0
4	64M	256	1536	510	8
16	256M	64	1920	126	32
64	1024M	16	2016	30	128
256	4G	4	2040	6	512
1024	16G	1	2048	0	2048

[0048] There are fairly many symbols which should be processed at this time of day as a migration terminal of a W-CDMA system actually, and supposing the number of antennas is two, when the signal which must be stored in the memory section per symbol as an input signal takes into consideration further a total of six multiple channels of control and traffic of a complex modulating signal (I/Q) and a delay wave component, the number of them is a total of 24-48.
[0049] In addition, since other base stations must be caught to a coincidence term at the time of DHO (tie rod city hand off), it doubles [the / one to]. 1 time, DHO is performed without making hardware increase by omitting the one section of the signal regeneration of the base station concerned while performing a current communication link, reducing numbers of passes, or carrying out **.
[0050] Moreover, the diffusion code is also formed into the complex modulation and, the case of the multi-code which changes a diffusion code further and is transmitted to this time of day, and in the case of the long code mask symbol of the first perch and the 2nd perch, it is necessary to perform actuation which makes an input signal the same, changes only a code, and obtains a correlation output.
[0051] therefore -- if it is going to acquire correlation using the usual SC -- the number of SC -- at least 96 to the four to 5 times -- about 500 are needed. Furthermore, in addition to this, although the searcher for obtaining a synchronization is required, the matched filter (MF) method is usually used for the searcher, and a hard scale becomes about 100 to 300 times compared with SC.
[0052] About 200 gates of gate numbers of SC are **(ed), and, specifically, the gate number of MF of operation precision is the abbreviation 60k gate extent need. However, since the operation precision for the data recovery of W-CDMA is not needed, actuation of a searcher will be sufficient with 10k gates extent. Moreover, one more may be needed, in order the searcher is required and to correspond for every antenna at the time of DHO.
[0053] In the above-mentioned situation, although the memory section and multi-tap F/F must be newly established if this circuit is used, it becomes possible to lessen the number of a high-speed correlator, and reduction of a large hard scale is possible. Furthermore, since it becomes unnecessary [the searcher for synchronous prehension] so that it may mention later, reduction of a still larger hard scale is brought about.
[0054] The memory section has enough usable DRAM (Dynamic Random Access Memory) of two ports etc., and if compared with the circuit constructed by digital F/F (Flip-Flop), reduction of a large chip occupancy area and **** of power consumption of it will become possible.
[0055] Although the actuation (at the time [Usually] of a communication link) after a symbol synchronization, a wireless slot synchronization, and frame synchronization are established was explained above next, the time of the initial synchronization which these synchronizations have not established is explained. At the time of an initial synchronization, it is in the condition which turned on the electric power switch of a migration machine, and a symbol synchronization, a wireless slot synchronization, and frame synchronization must not yet be established, but a synchronization must be specified in the condition. By the specification of ARIB, as it is the following, an initial synchronization is established.

[0056] As the 1st step, establishment a chip synchronization, a symbol synchronization, and wireless slot synchronous is performed. First, the long code mask symbol of the 1st perch is detected, and a chip synchronization, a symbol synchronization, and a wireless slot synchronization are established. Hereafter, as conditions for explanation, the chip rate of the 1st perch is set to 4Mcps(es), a diffusion coefficient is set to 256, and the signal input from A/D converter 11 is made into over sampling technique (16Mcps) and 6 bits 4 times.
[0057] And the configuration and actuation at the time of an initial synchronization are explained to the following (A) - (N). In addition, although explained based on the example of drawing 2 , the case of 16 times as many time amount conversion as this is explained especially concretely.
[0058] (A) The memory section 14 is taken as 1024 tap (6 bits is ********** image to 1024-piece width) +alpha (number tap).
(B) Write the output from A/D converter 11 in this memory section 14 one by one. Drawing speed uses a 16MHz clock.
[0059] (C) If it writes in 1024 taps (a part for one symbol [Exactly] of a perch channel) exactly, data will be transmitted to multi-tap F/F (F/F for time amount conversion)15 at once by 16 taps using a 16MHz clock. The sample data for 63 pieces is transmitted to the transfer and coincidence from the beginning of a symbol also at 63 delay F/F17. At this time, multi-tap F/F15 and delay F/F17, and the high-speed correlator 16 are operated with the clock rate of 256MHz. Moreover, the writing to the 16MHz memory section 14 is continued and advanced. In addition, although it indicated that sample data was transmitted to delay F/F17 from the beginning of a symbol, this is a simple assumption and is not not necessarily the beginning of a symbol.
[0060] (D) The high-speed correlator 16 carries out a sum-of-products operation with a 256MHz clock. The diffusion code at this time is a common short code.
[0061] It takes 16MHz time amount exactly that the data of 16 taps of multi-tap F/F15a are all transmitted. 16 data are transmitted in this time amount at one multi-tap F/F15b which will be involved memory section 14. Then, the 17th data are sent out from multi-tap F/F15b.
[0062] When this actuation is repeated 64 times, the correlation output in 64 sample points will be obtained from 64 high-speed correlators (SC) 16 by coincidence. This is held, and if it changes and outputs for every sampling time by time sharing (with 16MHz), an output equivalent to MF can be obtained.
[0063] Furthermore, the accumulation machine in SC16 is reset here, and it starts again from the above (C). At this time, the first sample data for 64 pieces is thrown away, and is transmitted to delay F/F17 and multi-tap F/F15 of 16 taps from the memory section 14 from the 65th data.
[0064] By repeating this big motion 16 times, it is set to 64(sample data for individual) x16(time) =1024, and the correlation output for 1024 samples can be taken in 1 symbol time amount. If the information on the memory section 14 is also thrown away by 64 samples, it memorizes newly by 64 samples and is updated completely.
[0065] All the diffusion codes inputted into the high-speed correlator (SC) 16 are common, and are inputted from the beginning of a symbol. In the case of the exaggerated 4 time sample, 1 tap eye will be common to a part for four samples, and will be inputted.
[0066] (E) Since the rate of the high-speed correlator 16 operates by 16 times of a sample rate, when it finishes acquiring 64 correlation for one sample, it will take 64 sample time exactly. It is at this termination time, and since it is writing in the memory section 14 at the rate of 16MHz, the new input data for 64 samples is incorporated.
[0067] (F) Since the long code symbol diffused in short code is inserted only once in ten symbols, it must be repeated by at least 10 symbols to discover the base station of No. 1 [about] (0.625ms / 10 symbol). In addition, this duration is not different from the case where the usual MF is used.
(G) In addition, although the memory section 14 is enough for a 1024 tap owner **** principle target, since it does not eliminate due to signal-processing delay, it has established allowances. What is necessary is to update by returning to 1 tap eye of the 1025 tap writing ******** beginning, and just to go.

[0068] (H) Thus, if it sees by at least 10 symbols, it is possible to take a wireless slot synchronization also including an adjoining base station from the location of the chip synchronization, symbol synchronization, and long code mask symbol of an enrollment base station. This processing is performed by the profiler and the logic which measures and detects the strongest correlation output, and its time amount are specified. Of course, if a communication link situation is bad, when it cannot judge only by the data for these ten symbols (equivalent to 1 wireless slot), a part for the ten following symbols will be doubled and judged. He carries out addition etc. and is trying to judge the result in the sample unit in phase within 1 wireless slot within a profiler. Anyway, what is necessary is just to repeat the above-mentioned data processing continuously.
[0069] Next, the power consumption in the correlation circuit for spread spectrum systems which the gestalt of operation of this invention requires is concretely explained using [Table 2], [Table 3], and drawing 3 . The clock frequency (MHz) of each example, the gate number of a high-speed correlator (SC), the gate number of F/F of the memory section, the gate number of delay F/F, the gate number of multi-tap (time amount conversion business) F/F, and the gate number that is the sum total further are shown for a 1 time as many conversion time as this, 4 times, 16 times, 64 times, 256 times, and 1024 times as an example of a-f.
[0070]
[Table 2]

		MHz	kゲート	kゲート	kゲート	kゲート	kゲート
	変換時間	クロック周波数	SC	メモリ部のF/F	遅延F/F	時間変換用F/F	合計
a		16	600	0	135	0	735
b		64	154	102	34	1	291
c	16	256	39	127	4	2	172
d	64	1024	10	133	1	8	152
e	256	4096	3	135	0	34	172
f	1024	16384	1	135	0	135	271

[0071] Moreover, the power consumption about the case of CMOS process level (gate length) 0.35micrometer, 0.25 micrometers, and 0.18 micrometers is expressed to the example of a-f. It is calculated with a (power consumption W) = gate number x frequency x unit power consumption value. Unit power consumption is expressed with muW/gate/MHz and offered by each manufacturer. In addition, [Table 3] also shows the power consumption of 600k gates full MF to reference.
[0072]
[Table 3]

	消費電力 (W)		
	0.35μm	0.25μm	0.18μm
a	7.06	0.82	0.41
b	8.22	0.96	0.48
c	8.15	0.95	0.48
d	13.23	1.54	0.77
e	91.72	10.72	5.36
f	1339.88	156.32	78.16
フルMF	5.76	0.67	0.34

[0073] moreover -- if the power consumption of 0.25 micrometers of gate length in [Table 3] is indicated by Log -- the example of a-f -0.08449, -0.01825, -0.02198, and 0. -- it is set to 188364 and 2.194013 and the change is expressed to drawing 3 . Drawing 3 is drawing showing the Log display of the power consumption of 0.25 micrometers of gate length. In this drawing 3 , it turns out that the case (1 to 16 times as many conversion time as this) of a-c serves as a low power.
[0074] Next, specification of a long code group is explained as the 2nd step. If the synchronization of a wireless slot is establishable, since it turns out where the long code mask symbol of the 2nd perch exists, the information will be incorporated in memory. In fact, since it exists in the same location as the long code mask symbol of the 1st perch, the information to acquire will be acquired in the same location.
[0075] And 1 sample eye which incorporated the information incorporated in memory in the memory section 14 since the symbol synchronization was established in this case, although what is necessary is just to have performed for example, actuation [at the time of an initial synchronization] (A) - (C) is surely the head of a symbol. Then, since correlation will be acquired by either if the information read from the memory section 14 is processed by exchanging not the same diffusion sign as a high-speed correlator but 16 kinds of diffusion signs, a long code group can be specified.
[0076] It is very easy to attain specification of this long code croup within 1 symbol time amount. Since the correlation output of 64 figures is obtained by coincidence within 64 sampling times as the precedent described, delay F/F17 is necessarily unnecessary in this case. It is more suitable to supply the same signal to 64 high-speed correlators (SC) 16.
[0077] Next, specification of a long code and establishment of frame synchronization are explained as the 3rd step. If the synchronization of a wireless slot is establishable, since it turns out where the pilot symbol of the 1st perch exists, the information is incorporated in the memory section. Information may also be shortly incorporated by two symbols, and if there is idle memory, you may make it incorporate by 4 of all pilot symbols symbols.
[0078] If incorporation of information is completed, it will carry out like the case where it is the 2nd step. In all the class of long code including phase contrast in 1 long code croup 32 kinds, Since a phase becomes the repeat of 16 wireless slot and 16 kinds exist Even if it carries out by exchanging a long code with one correlator It can specify in 32(32 kinds) x16(16 phases) x4(pilot wave for four symbols) x4([1 sample is time amount of 16MHz] by 64 samples with 4 microseconds : 256MHz clock) /64=128microsecond (since the correlation output of 64 pieces is obtained by coincidence).
[0079] If specification of a long code is performed in the real time using the usual correlator Since a pilot symbol exists in ten symbols only 4 times at 1 symbol time amount (64 microseconds) x32(32 kinds) x16(16 phases) =32768microsecond (about 33ms), Since it becomes this thing 2.5 (10/4) or more (about 33msx 2.5) twice, i.e., 80ms, if this circuit is used as compared with the conventional correlator, large time amount compaction is possible.
[0080] Hereafter, the duration in each step in an ideal condition is written. Conditions are considered as the case where a 1GHz clock is usable.
The 1st step: 0.625ms (the same as that of the conventional method)
The 2nd step: 0.001ms (the conventional method 1 wireless slot 0.625ms)
The 3rd step: 0.2ms (the former 80ms)
[0081] Actually, since 1 wireless slot is necessary to one processing, it writes per wireless slot.
The 1st step: 1 (the same as that of the conventional method)
The 2nd step: 1 (the same as that of the conventional method)
The 3rd step: 1 (in the former, it is set to 32x16=512 (512 wireless slot x0.625ms=320ms), and in order to process still more correctly, it will take this 4 to 5 times.)
Anyway, if it would compare with the conventional method even if the time amount of the 3rd step is main, and it raises the single figure time amount of the 1st step, since the time amount of the 3rd step is sharply shortened in this circuit, in addition, it would win.
[0082] Next, the actuation at the time of DHO (diversity hand-over or diversity hand off) is explained. By the case where communication environment with the base station (the present base station) which is performing the present communication link gets worse (when it becomes the situation of having

approached the base station (contiguity base station) which keeps away from the base station where the case where they are many is communicating, and approaches) Although a contiguity base station is discovered first and communication with the contiguity base station is begun when communication environment with it better [to carry out the communication link with a contiguity base station] is acquired, I have the same information as the information from the present base station sent from a contiguity base station, and both are received. That is, cel diversity reception is performed, it continues until the level of both input signals becomes beyond a predetermined value, and the communication link with the present base station is cut after that, and it shifts to a communication condition with a new adjoining base station. Communication which does not have software hand-over, a software hand off, a call, and a break in this is enabled. Thus, it is DHO to perform cel diversity reception and to perform software hand-over or a software hand off.

[0083] By the specification of ARIB, all base stations are asynchronous and are operating. Therefore, the processing as the case of the above-mentioned initial synchronization that the process in which the chip synchronization of an adjoining base station, a symbol synchronization, and a wireless slot synchronization are established is the same is needed. Therefore, newly extending hardware is usually performed to DHO. A part for one antenna is specifically used independently, and it is turned to a contiguity base station, or the measures against a thing are taken. [0084] which describes the method which uses hard empty time amount here and performs DHO In addition, even if it is the hard configuration of not supporting Book DHO, as mentioned above, the slide correlator of a large number which carry out inverse transformation (recovery) of the information to much memory is installed. When a migration machine carries out switch-on of the max of these numbers, it is a time of catching a perch channel, and if the actuation is completed, many will become good [a memory or slide correlator] at hibernation. If it is used at the time of DHO, it can restore to the information from the base station of the hand-over point satisfactory.

[0085] Next, this circuit is explained using drawing 4 and drawing 5 about the case where it uses as an interference canceller. Drawing 4 is the configuration block Fig. which used the correlation circuit concerning the gestalt of operation of this invention for the interference canceller unit. Drawing 5 is the configuration block Fig. of an interference canceller using the interference canceller unit concerning the gestalt of this operation. The interference canceller unit (ICU) was equipped with MF as the configuration was shown in drawing 4 , and further, since the interference canceller consists of many ICUs as shown in drawing 5 , it has brought about increase of an LSI scale, and increase of the LSI number.

[0086] MF of a number of number of users x stages x integral multiple is required, at least 3 is needed and, specifically, as for an integer, MF of at least 4 or 8, therefore 3000-10000 is needed [as for 300 or 600, and the number of stages] for the number of users. In the gestalt of this operation, this circuit in which high-speed data processing is possible is carried out in the above-mentioned MF section, and the number of MF is reduced sharply.

[0087] Moreover, as shown in drawing 5 , the memory section and multi-tap F/F are prepared in the latter part of a receive section (RX) and two adders (+), and time amount conversion of processing speed is performed between an adder and two or more ICUs between an adder, a delay circuit, or two or more ICUs between ********, a delay circuit (Delay), or two or more ICUs. Therefore, the matched filter (MF) shown in drawing 4 processes a high-speed sum-of-products operation compared with the usual MF.

[0088] In addition, it is in the correlator which used that it read it by many taps and performed time amount conversion in a logical circuit (F/F) after the fundamental concept of this patent accumulates CDMA modulation information in memory, and although the following concepts are incorporated, there is no change in the effectiveness.

(1) Reduction of a clock rate with high-speed read-out using a high-speed correlator, and the multilayer clock in the case of an operation. In this case, since the number of a high-speed correlator increases, it is not directly connected with reduction of power consumption.

(2) Adjustable [of the multiple of over sampling technique]. An initial state is increasing 4 times, after

******(ing) and carrying out outline decision etc. 2 double.
(3) When a high-speed correlator and MF (sum-of-products computing element) configuration are used as a complex mold. Like drawing 8 , although theoretically constituted by four high-speed correlators, by devising, a complex high-speed correlator (complex mold high speed SC) becomes less than 4 times, and can constitute a hard scale on a scale of twice [about]. In addition, drawing 8 is a circuitry block diagram at the time of using the high-speed correlator in the spectrum diffusion communication circuit concerning the gestalt of operation of this invention as a complex mold. However, in drawing 8 , in one complex mold high speed SC, this is the preceding paragraph of a correlator, in order to perform addition and subtraction of I which carried out the multiplication of the diffusion code, and a Q signal, it becomes unnecessary to use four correlators for the correlator being two pieces about four I and Q signals, and processing of it is attained with two correlators.
[0089] That is, in the case of complex multiplication, time amount addition as shown in the following formulas is performed.
(AI +jAQ)(CI +jCQ)=AI CI -AQ CQ +j(AI CQ +AQ CI)
Although time amount addition of AC is performed in one correlator when not being complex Although four correlators are theoretically needed when in a complex case it is originally made to subtract and add using four correlators, after performing time amount addition of AI CI, AQ CQ, AI CQ, and AQCI At the example shown in drawing 8 , it is AI CQ+AQCI as AI CI-AQ CQ. After calculating, if time amount addition is performed, reduction of a hard scale will be enabled.
[0090] When the contents of drawing 8 are explained, in addition, the configuration in the case of a complex mold Input a spectrum diffusion signal and the 6 bitA/D converter 81 which changes an analog signal into a digital signal is formed corresponding to I phase signal and Q phase signal. The memory section 82 holding the digital signal outputted from this 6 bitA/D transducer 81, Multi-tap F/F84 which reads and carries out parallel/serial conversion of the data from the memory section 82 by many taps (many samples) is formed, respectively. Furthermore, two or more latch circuits 83 which adjust the timing of the signal of the data inputted into the complex molds 80a, 80b, and SCs 80c, and a code and others with a clock (CLK) are formed.
[0091] According to the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention A/D conversion of the input signal by which spectrum diffusion was carried out is carried out with the 16MHz clock of an exaggerated sample 4 times. In the memory section Part extent writing for one symbol, While reading it to multi-tap F/F by many taps and carrying out multiple-times sending out of the data for one symbol with a 1.6GHz - 16GHz 100 to 1000 times as many clock as this Since the high-speed correlator is made to perform high-speed data processing for the data for one read symbol, writing the data for the one following symbol in the memory section, it is effective in the ability to make a configuration element number small-scale and obtain a correlation output.

[Translation done.]

EXAMPLE

[Example] Next, the concrete and fundamental circuitry of the recovery section using this circuit is explained using drawing 6 . Drawing 6 is the concrete configuration block Fig. of the recovery section of the correlation circuit for spread spectrum systems concerning the example of this invention. The recovery section of this example consists of fundamentally an antenna 51, the RF section 52, A/D converter 53, the memory section 54, multi-tap F/F63, the 1st high-speed correlator 55, the diffusion coder 56, a profiler 57, the 2nd high-speed correlator 58, the RAKE composition machine 59, data and the speech processing section 60, a control section 61, and finger memory 62, as shown in drawing 6 .
[0093] Next, each part of the recovery section shown in drawing 6 is explained concretely. Two antennas 51 are usually prepared and perform diversity reception. Diversity reception compounds the result to which received the same sending signal with two antennas, and it restored, and improvement in receiving sensibility is aimed at.
RF [0094] The RF (Radio Frequency : radio frequency) section 52 creates a baseband (BB) signal (recovery), performs rectangular detection, and divides it into I component (inphase component) and Q component (orthogonal component).
[0095] A/D converter 53 changes BB analog signal from the RF section 52 into a digital signal. 4-6 bits of conversion numbers of bits are required. 4 times, if a conversion frequency is over sampling technique, in the case of W-CDMA (wideband CDMA), it will be set to 16MHz. Although it receives for every I/Q signal, and antenna and one A/D converter is needed, respectively, if high-speed processing is possible, it will be sufficient to make time-sharing processing perform with one A/D converter.
[0096] The memory section 54 holds above the digital signal changed with A/D converter 53 by at least 1 symbol. Although about 1 to 4 times of a chip rate and the read-out rate of drawing speed may also be the same, read-out is performed by many taps. Multi-tap F/F63 carries out serial conversion of the data inputted by the parallel of many taps from the memory section 54, and outputs them to a high-speed consecutive correlator. Here, time amount conversion will be performed. In addition, when using MF (matched filter) instead of a high-speed correlator, simultaneous read-out by the symbol unit is required. Moreover, it has memory section 54' as an object for DHO.
[0097] The 1st high-speed correlator (Digital SC) 55 incorporates the signal and the diffusion sign from the diffusion coder 56 which are held at the memory section 54 and by which spectrum diffusion was carried out, and performs the sum-of-products operation per 1 symbol. High-speed operation is performed compared with a chip rate. Moreover, although the actuation as the 1st high-speed correlator 55 also with the 2nd same high-speed correlator (Digital SC) 58 is performed, the result of an operation of the 2nd high-speed correlator is outputted to a profiler 57. In addition, you may make it use a matched filter (MF) instead of the 2nd high-speed correlator 58. Moreover, it has high-speed correlator 58' as an object for DHO.
[0098] The diffusion coder 56 is sent out with the phase which had the specified diffusion sign specified by the directions from a control section 61. In addition, you may be the register which stores a diffusion sign instead of a diffusion coder. As long as it is the diffusion coder of the usual rate, it may incorporate

in the memory section like processing of a CDMA modulating signal, and time amount conversion may be carried out by multi-tap F/F, it may incorporate to multi-tap F/F directly, and high-speed time amount transform processing may be carried out. It is better to incorporate to multi-tap F/F directly, since there is little number of bits and it uses rather in many cases, repeating the same sign.

[0099] A profiler 57 calculates by incorporating the output from the 2nd high-speed correlator 58 (or MF), and specifies pass. Thereby, in the phase of an initial synchronization, a chip synchronization, a symbol synchronization, a wireless slot synchronization, and frame synchronization can be taken, and pinpointing of a base station is attained. Moreover, pass is detected in the communication link condition it was decided that a connection place base station would be. Such information is sent to a control section 61, and directions are outputted to the 1st high-speed correlator 55, the memory section 54, and the diffusion coder 56 from a control section 61. Moreover, as an object for DHO, it has profiler 57' and specification and specification of pass of an adjoining base station are performed at the time of DHO.

[0100] The signal with which spectrum diffusion of the MF used instead of was carried out and a diffusion sign are incorporated, and the sum-of-products operation is performed per 1 symbol. [the 2nd high-speed correlator 58] High-speed operation is performed compared with a chip rate. Since the information from two or more memory can be extremely processed at a high speed by carrying out high-speed operation, the application to an interference canceller is attained.

[0101] The RAKE composition section 59 carries out phase correction [output / from the 1st high-speed correlator 55 incorporated by the finger memory 62 / correlation] using a pilot symbol, and performs composition (RAKE composition) of two or more pass after that. Moreover, **** rare **, such as a SIR test section which, in addition to this, measures what has happened to AFC for doubling an input signal and a frequency, the input signal, and the noise (the interference from other signals is included) comparatively or or now in the RAKE composition section 59.

[0102] Data and the speech processing section 60 perform inverse transformation (recovery) of various signal processing carried out by the transmitting side in order to perform an error correction. this -- a day interleave, Viterbi decoding, a CRC decoder, the Lead Solomon double sign (or turbo decode), and voice -- CODEC -- ** -- it ******.

[0103] As mentioned above, according to the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention, the demodulator circuit of CDMA can be constituted on a scale of little gate, it is small-scale to the near future, and the effectiveness that LSI for mobile terminals from which correlation is acquired can be developed is in it as explained to the detail.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the configuration block Fig. of the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention.
[Drawing 2] It is the configuration block Fig. of another correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention.
[Drawing 3] It is the graphical representation having shown the situation of the power consumption in this invention.
[Drawing 4] It is a configuration block Fig. at the time of using this circuit for an interference canceller unit.
[Drawing 5] It is a configuration block Fig. at the time of using this circuit for an interference canceller.
[Drawing 6] It is the configuration block Fig. showing concrete 1 example of the circuit for spread spectrum systems concerning the gestalt of operation of this invention.
[Drawing 7] It is the configuration block Fig. of another correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention.
[Drawing 8] It is a configuration block Fig. at the time of using the high-speed correlator in the correlation circuit for spread spectrum systems concerning the gestalt of operation of this invention as a complex mold.
[Drawing 9] They are some configuration block Figs. of the conventional slide correlator.
[Drawing 10] It is the configuration block Fig. of the conventional matched filter.
[Description of Notations]
11, 31, 41 -- A/D converter 12 -- Control section 13 -- Code generator, 14 -- Memory section 15 -- Multi-tap F/F 16 -- A high-speed correlator, 32 42 -- Multiplier 33 43 -- PN code register 34 44 -- Adder, 35 -- Delay circuit 45 -- Sample hold (S/H) circuit 51 -- Antenna, 52 -- The RF section 53 -- A/D converter 54 -- Memory section, 55 -- 1st high-speed correlator 56 -- Diffusion coder 57 -- Profiler 58 -- 2nd high-speed correlator 59 -- RAKE composition section 60 -- Data and the speech processing section 61 -- Control section 62 -- Finger memory 63 -- Multi-tap F/F

[Translation done.]

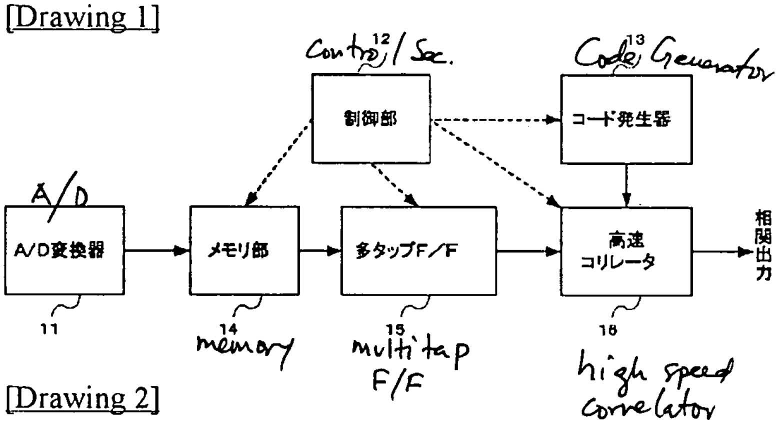
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

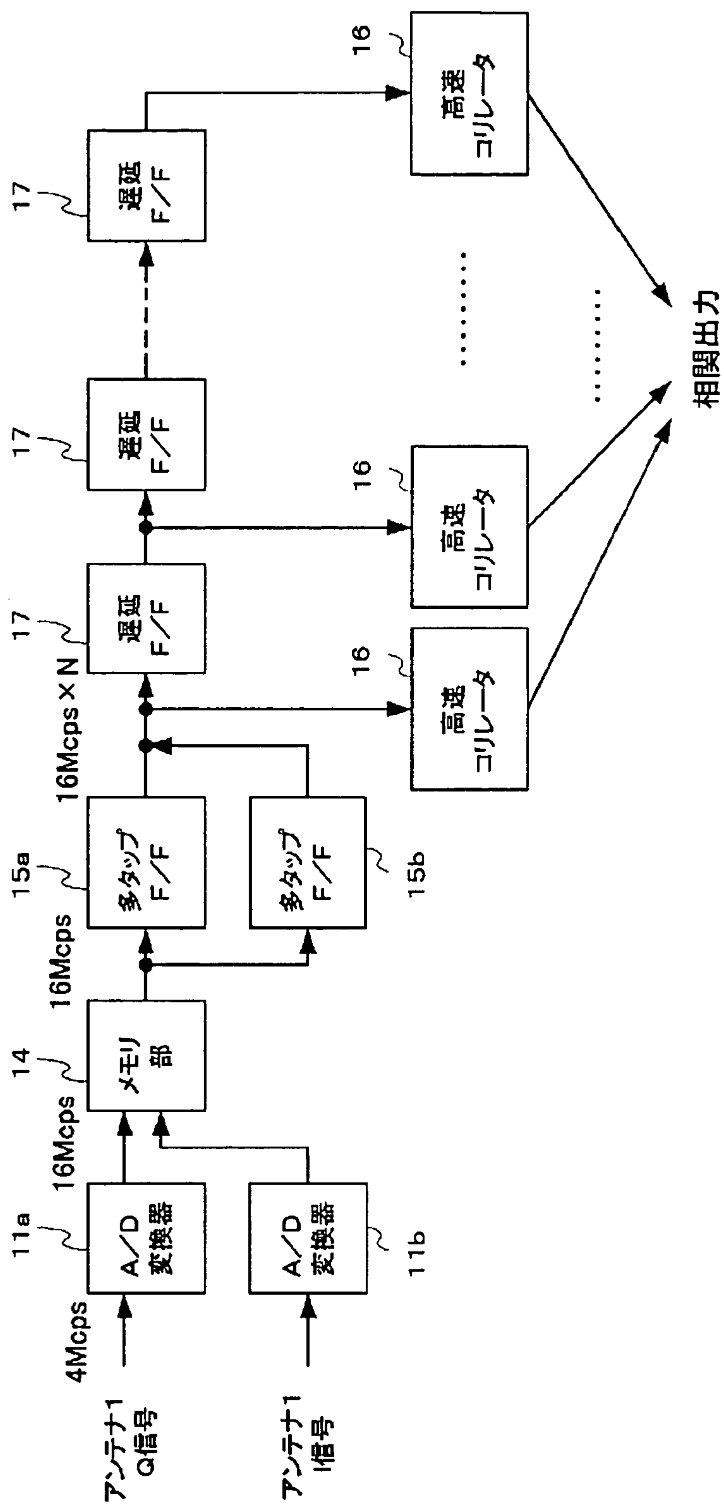
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

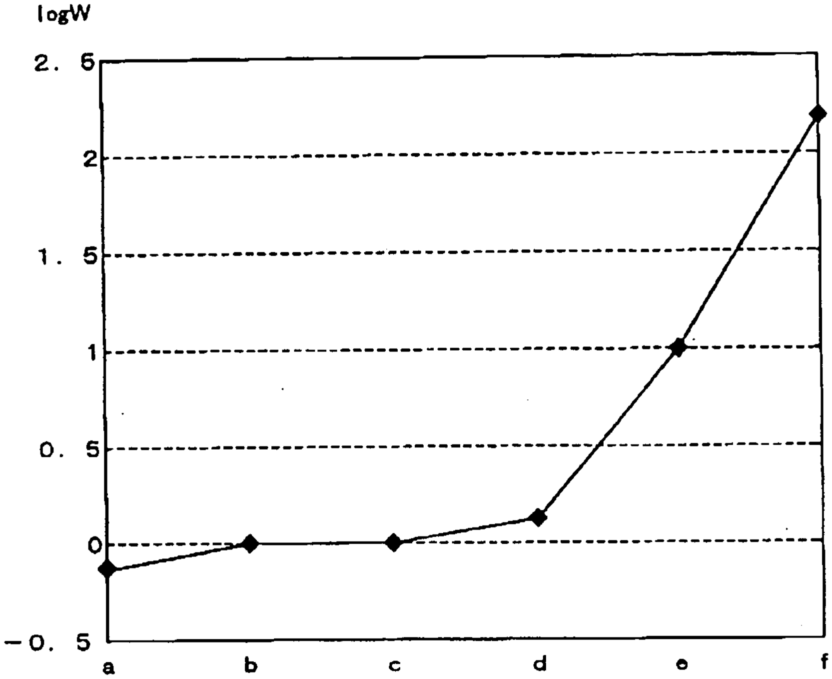
[Drawing 1]



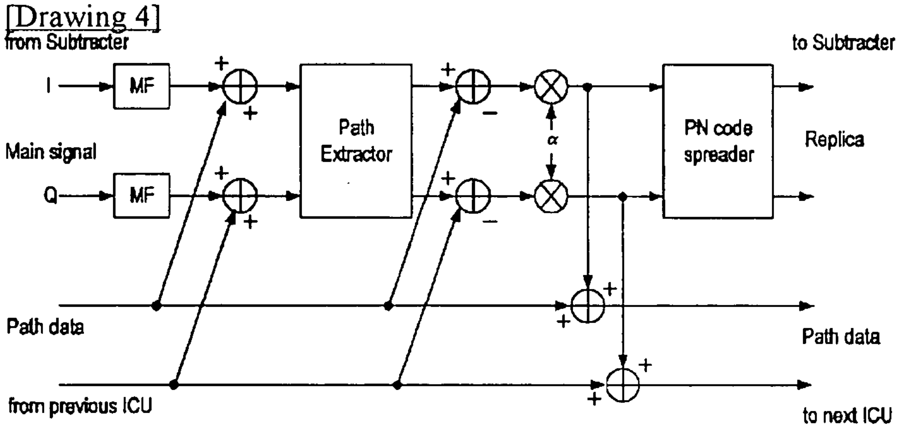
[Drawing 2]


アンテナ1
Q信号
アンテナ1
I信号
4Mcps
A／D
変換器
11a
11b
16Mcps
メモリ
部
14
16Mcps
多タップ
F／F
15a
15b
16Mcps×N
遅延
F／F
17
高速
コリレータ
16
相関出力

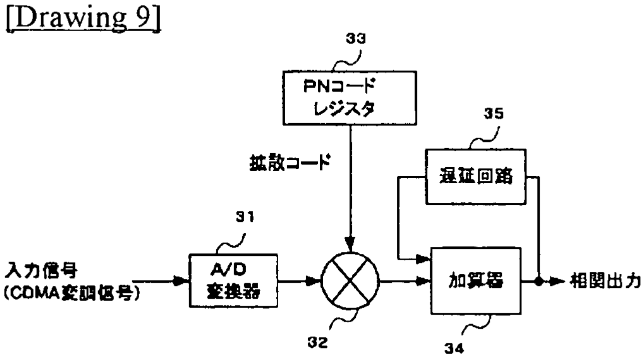
[Drawing 3]



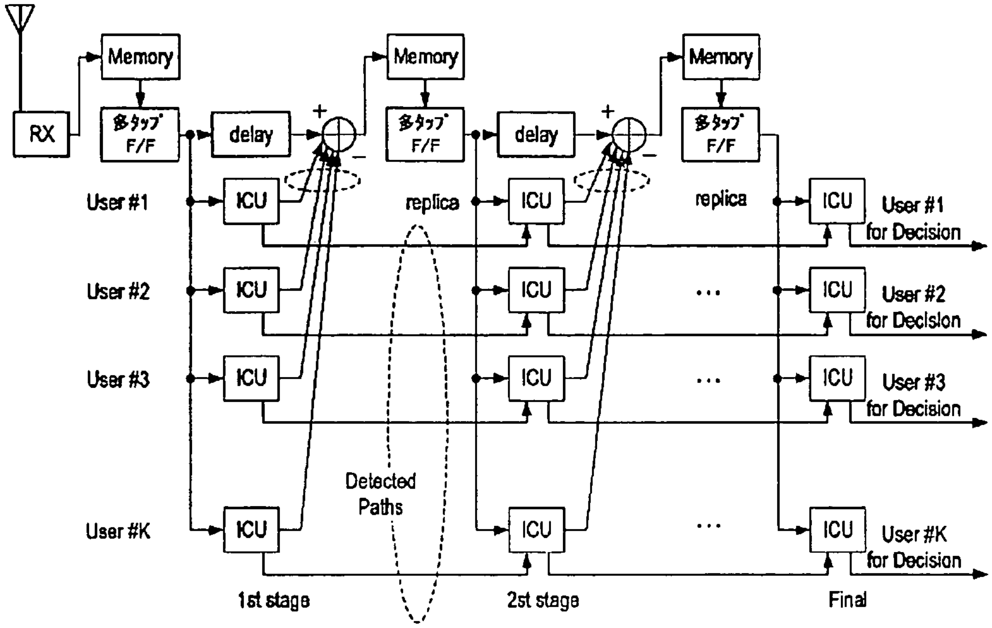
[Drawing 4]



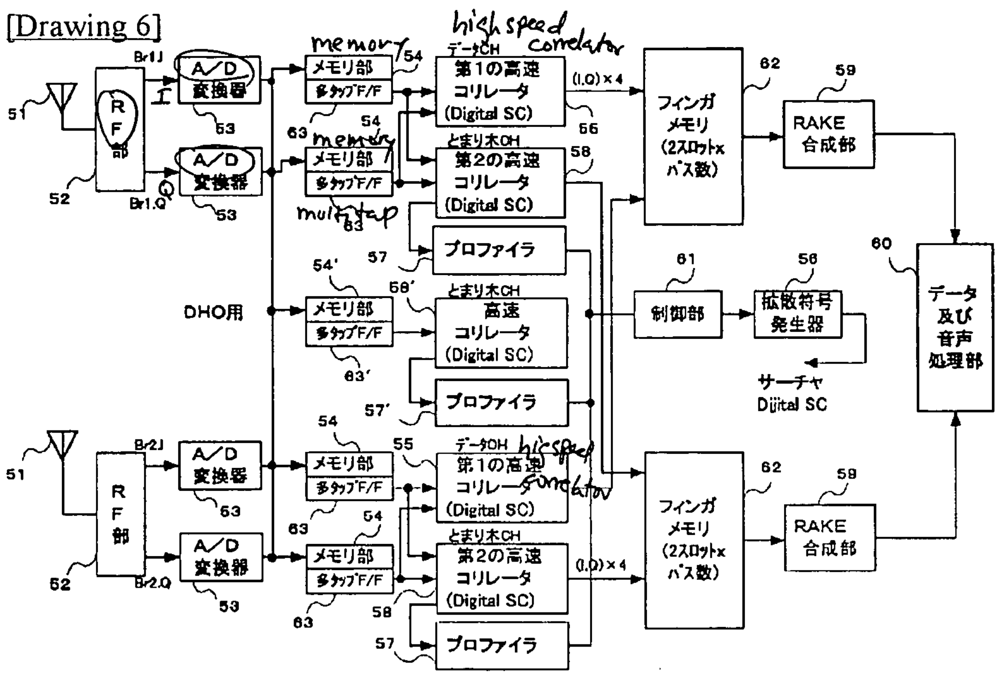
[Drawing 9]



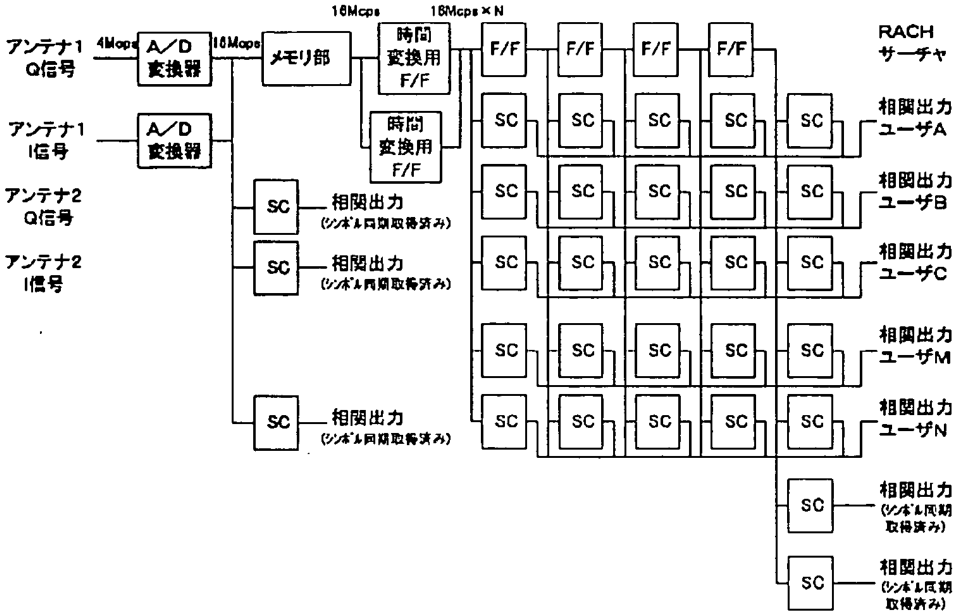
[Drawing 5]



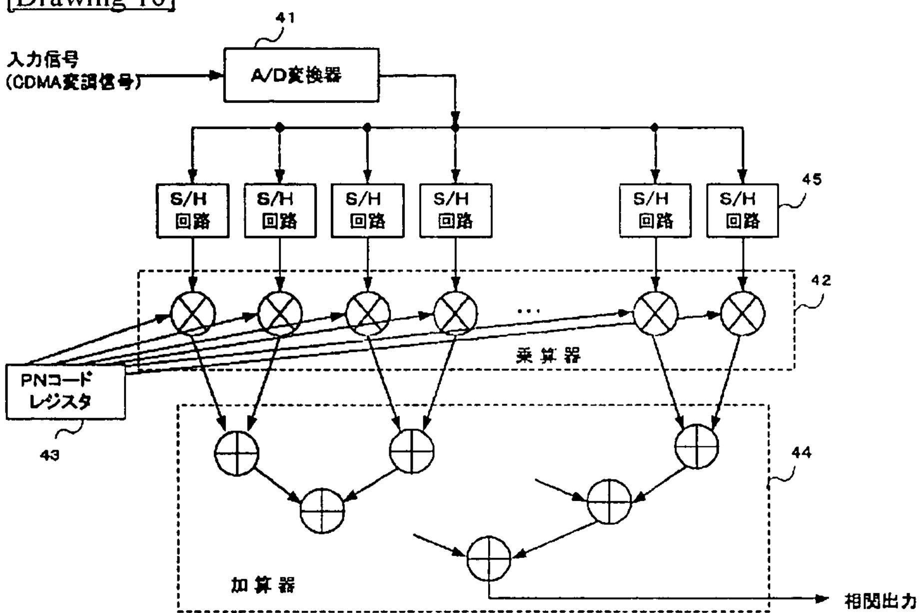
[Drawing 6]



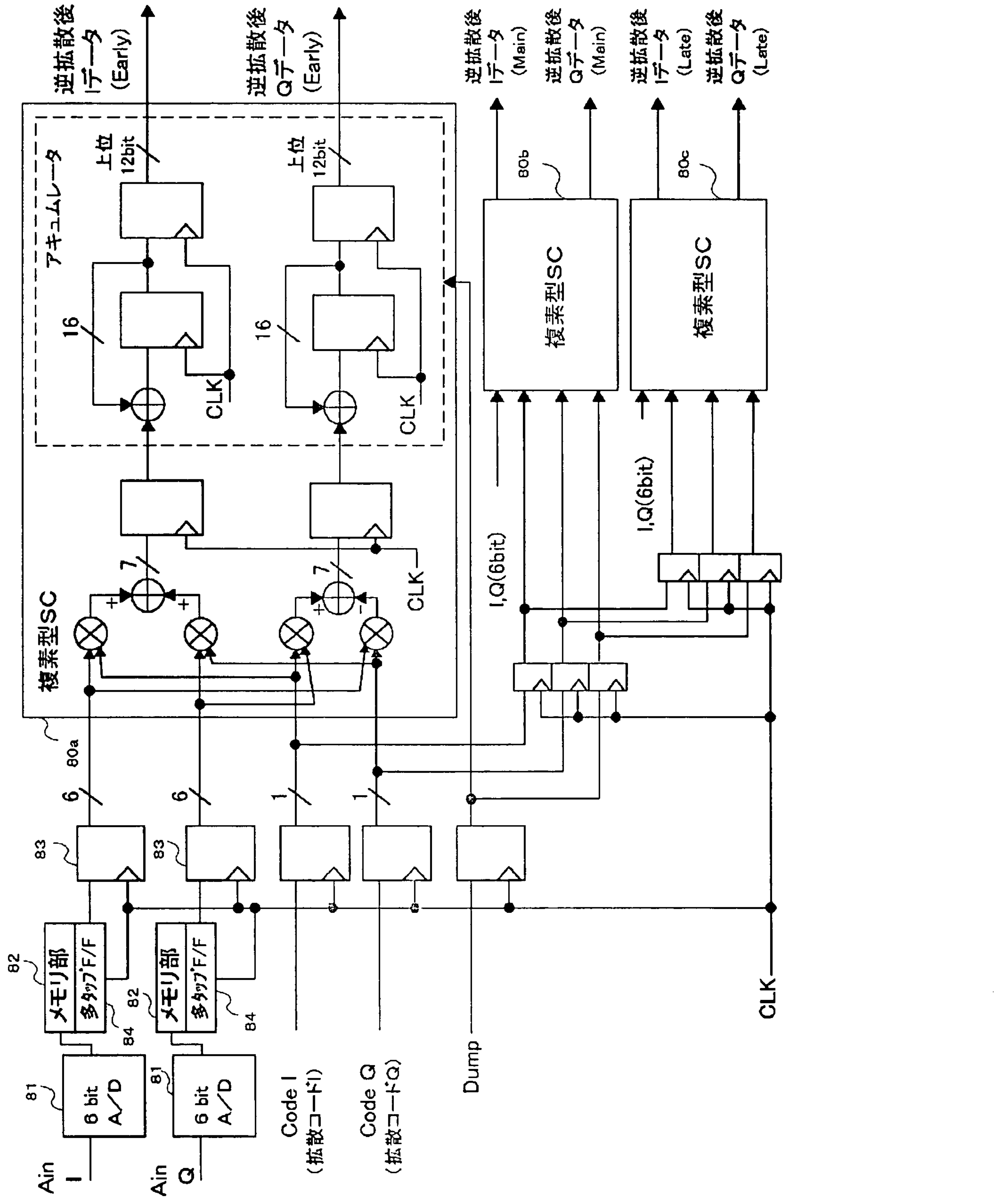
[Drawing 7]



[Drawing 10]



[Drawing 8]



[Translation done.]